A Single Phase Boost Converter Based Five Level Inverter

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Abstract **- Nowadays Multilevel Inverters are in high demand for high power, medium voltage applications. The proposed 5 level inverter uses a DC source and minimum count of switches so that the total cost and complexity of circuit is reduced. It has the ability of boosting the output voltage to high level. Multicarrier Pulse Width Modulation (PWM) technique is implemented in the presented topology and output voltage waveform across load by connecting filter components and without connecting filter components are analyzed using power electronics tool box of MATLAB. Also variation of Total Harmonic Distortion (THD), RMS output voltage and Peak output voltage are compared for proposed inverter by connecting filter components and without connecting filter components for various values of modulation indices.**

Index Terms **-** *Multicarrier; Modulation; THD; PWM; Boost*

I. Introduction

General inverters are two level converters and they cannot satisfy high power applications. Multilevel inverters are preferred to satisfy high power applications. Multilevel inverters are used to produce very high voltages based on the configuration used even from a single DC voltage source. Whenever the no of levels of Multilevel inverters are increased, Total harmonic distortion (THD) of output voltage is reduced which is suitable for numerous applications. So the filter requirement is reduced when multilevel inverters are used for applications.THD can also be reduced in lower levels when suitable modulation techniques are used. When low switching frequency Pulse Width Modulation techniques (PWM) are used, THD value will be very high. But Multicarrier PWM techniques reduce the amount of total harmonic distortion. The general topologies of multilevel inverters are Diode clamped multilevel inverter, flying capacitor multilevel inverter and Cascaded Multilevel inverter. Conventional topologies use more no of switches, capacitors and diodes. Each and every type has its own advantages and disadvantages. The proposed topology has less no of switches and uses a single DC source. Capacitors are used instead of other DC sources. Since less no of switches and DC sources are used, the overall weight and cost of the configuration is reduced. The suggested topology has the ability to boost the input voltage and produces high output voltage. Two switches in the presented topology are operated at low switching frequency, which in turn reduces the switching stress and switching losses. The only drawback is the proposed topology uses more no of inductors and capacitors, which may increase the size of the configuration. Taghvaie et al [1] proposed a structure of Multilevel Inverter, which uses switched capacitors and DC sources. He introduced a self-balanced asymmetrical charging pattern in the work. Reddy and Pattnaik [2] proposed a Multilevel Inverter topology, which can be operated under symmetrical & asymmetrical configurations. Sureshkumar et al [3] discussed about a new circuit with minimum count of switches for different carrier PWM techniques. Mufeeda and GeethuKrishnan [4] suggested an Asymmetric Multilevel Inverter which has reduced number of switches for a 11 level inverter and a comparison was made between fundamental and high frequency control. Mehdi Fallah et al [5] evaluated the performance of a new structure for cascaded H-Bridge based modular multilevel voltage source inverter. Muhammad Arif et al [6] designed a multilevel inverter of 5 level and THD is analyzed for various multicarrier PWM control schemes. Vanya Goel et al [7] proposed a 5 level inverter which can give high step up output voltage. Vanya Goel et al [8] evaluated THD results for the proposed 7 level inverter which employs level shifted PWM technique. Deepa and Rakesh Kumar [9] suggested a new circuit topology named one two five topology for asymmetrical multilevel inverter and the harmonics are reduced using sine property. Amir Taghvaie et al [10] proposed a new multilevel inverter circuit which uses single DC source and capacitors are used instead of other DC sources. Kishor Thakre and Kanungo Barada Mohanty in [11] made a comparative analysis of THD of a symmetrical and asymmetrical 17 level cascaded H-Bridge inverter. Balamurugan et al [12] made a survey on various multilevel inverters and compares various topologies of multilevel inverters. Yuanmao et al [13] designed a structure based on switched capacitor technique and it avoids capacitor voltage balancing. Kanimozhi and Geetha [14] made an investigation about new boost switched capacitor topology for different

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multicarrier based PWM techniques. Bhuvaneswari et al [15] made a comparison of 3 phase cascaded multilevel inverters for different multicarrier sinusoidal PWM techniques. Balamurugan et al [16] also made a performance evaluation of three phase asymmetrical multilevel inverter with reduced switch count. Balamurugan et al [17] proposed an investigation on Z-source based three level inverter.

II. POWER CIRCUIT DIAGRAM FOR THE PROPOSED INVERTER

The circuit topology for the proposed 5 level multilevel inverter is shown in fig.1.It uses less no of switches and DC sources compared to conventional topologies. Other DC sources are replaced by capacitors. Since it uses less no of switches, the complexity of control circuit is reduced. The size of the circuit also reduced because of less no of sources. It consists of a boost converter unit and 2 no of diode capacitor cells (C1-D2 and D3-C2), which are used to boost up the input DC voltage.

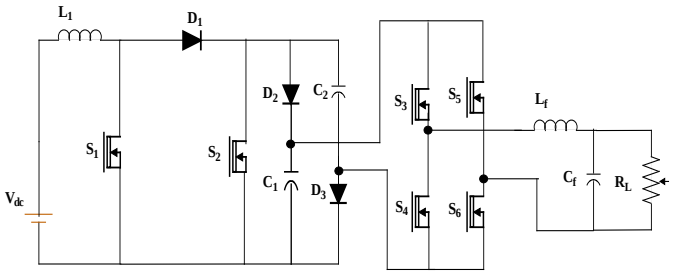

Fig.1. Power circuit diagram of proposed inverter.

Switches S3, S4, S5 and S6 form the polarity generating part of the circuit.S3 and S6 is responsible for generating positive output voltage and S4, S5 for generating negative output voltage. The boosted input voltage is available across the diode capacitor cell. After processed through polarity changing unit, multilevel output is available across the load. Switching states of different switches and diodes of a proposed inverter is shown in table1.

Parameters chosen for the proposed inverter are given below.

Switches S1 to S6	-	Ideal Switches
Diodes D0, D1, D2	-	Power Diodes
Capacitors C1=C2	=	330µf
Filter capacitor Cf	=	38µf
Filter inductance Lf	=	0.8H
Input Inductance L1	=	2mH
Load resistance RL	=	200Ω
Input voltage Vdc	=	100V
Switching frequency	=	1 KHz

III. MODULATION CONTROL TECHNIQUES OF MULTILEVEL INVERTER

The suggested multilevel inverter is performed using multicarrier modulation technique. There are two types of multicarrier modulation techniques available. They are phase shifted and level shifted modulations. Compared to level shifted modulation, phase shifted modulation generates more THD. Level shifted modulation again classified into three types. They are Phase Disposition PWM (PDPWM), Phase Opposition Disposition PWM (PODPWM), Alternate Phase Opposition Disposition PWM (APODPWM).The presented topology uses Phase Disposition PWM to get better THD. In level shifted modulation technique, for getting an "m" level output voltage of multilevel inverter it needs m-1 triangular carrier signals. All the carriers have same amplitude and frequency. Different types of level shifted PWM are discussed below with model waveforms.

A. PHASE DISPOSITION PWM (PDPWM)

In Phase Disposition PWM, all the carriers are in phase with each other. For an "m" level output voltage of multilevel inverter it needs m-1 triangular carrier signals. Since the proposed inverter is a 5 level inverter it needs 4 carriers, where two of them are available above zero axis and remaining two carriers are below zero axis. By comparing the carriers with the sinusoidal reference waveform high switching frequency pulses for various switches are generated. The reference and carrier arrangement of PDPWM method is shown in fig.2.

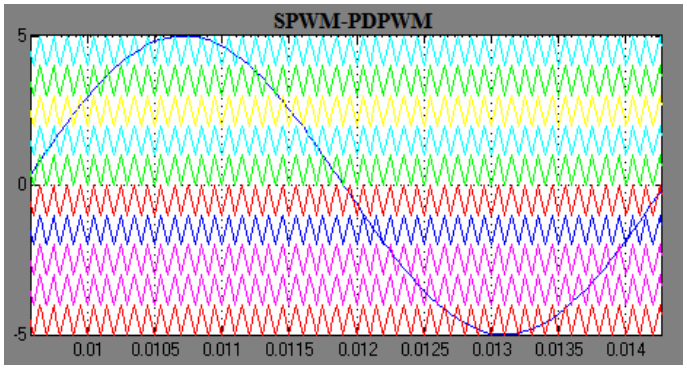

Fig.2. Sample reference and carrier arrangement of PDPWM

B. PHASE OPPOSITION AND DISPOSITION PWM (POPWM)

In Phase Opposition Disposition PWM, all the carriers above zero reference axis are 180deg out of phase with the carriers below zero axis. For a "m" level output voltage of multilevel inverter it needs m-1 triangular carrier signals. Triangular carrier signals are compared with the sinusoidal reference waveform and thereby high switching frequency pulses for various switches are generated. The reference and carrier arrangement of PODPWM method is shown in fig.3.

S.No	S_1	S_2	S_3	S_4	S_5	S_6	D_0	D_1	D_2	Level
1	SW	0	SW	0	0	1	0	0	0	First
2	SW	SW	1	0	0	1	1	1	1	Second
3	SW	0	0	1	SW	0	0	0	0	First
4	SW	SW	0	1	1	0	1	1	1	Second

TABLE I. SWITCHING PATTERNS AND STATES OF SWITCHES AND DIODES FOR EACH VOLTAGE LEVELS

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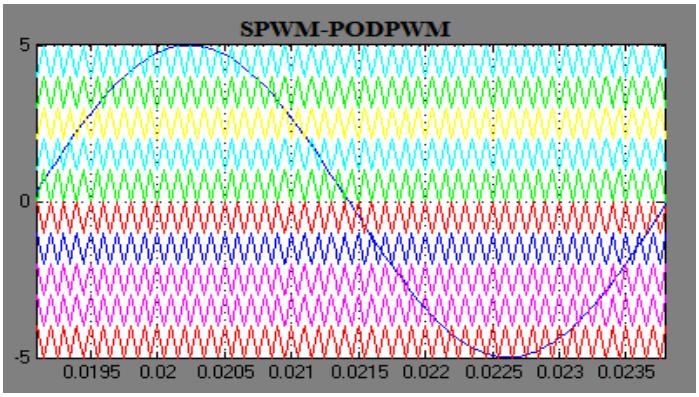

Fig.3. Sample reference and carrier arrangement of PODPWM

C. ALTERNATIVE PHASE OPPOSITION AND DISPOSITION PWM (APODPWM)

In Alternate Phase Opposition Disposition PWM, Each and every carrier is 180 deg out of phase with the adjacent carrier. Odd carriers are in phase with each other; similarly even carriers are in phase with each other. But odd carrier signals are 180deg out of phase with even carrier signals. Here also for a "m" level output voltage of multilevel inverter it needs m-1 triangular carrier signals. Triangular carrier signals are compared with the sinusoidal reference waveform and thereby high switching frequency pulses for various switches are generated. The reference and carrier arrangement of APODPWM method is shown in fig.4.

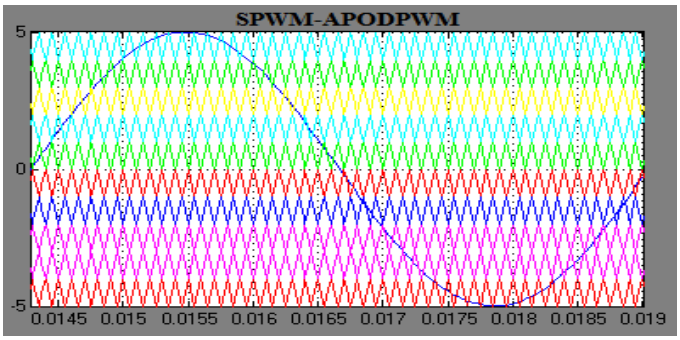

Fig.4. Reference and carrier arrangement of APODPWM

IV. SIMULATION RESULTS

The proposed 5 level MLI is constructed and simulated using MATLAB/SIMULINK. The output voltage waveforms for different modulation indices are analyzed. THD, Peak values of voltage (Vpeak), RMS output voltage (Vrms) are noted for various modulation indices with and without using filter are tabulated below in table 2.

TABLE II. COMPARISON OF THD, V_{PEAK}, V_{RMS} FOR DIFFERENT VALUES OF MODULATION INDEX

S.No	MI	THD(%)		Vpeak(v)		Vrms(v)	
		Without filter	With filter	Without filter	With filter	Without filter	With filter
1.	1.1	22.89	9.73	1210	115	855.4	814
2.	1	26.31	9.97	1176	1129	831.3	798.6
3.	0.95	29.3	10.02	1148	1114	811.4	787.9
4.	0.9	31.51	10.08	1121	1102	792.6	778.9
5.	0.8	36.78	15.84	976	738.3	690.2	522.1
6.	0.75	39.44	16.12	897.7	682.7	634.8	482.7

The Simulink model of discussed MLI is shown below in fig.5.

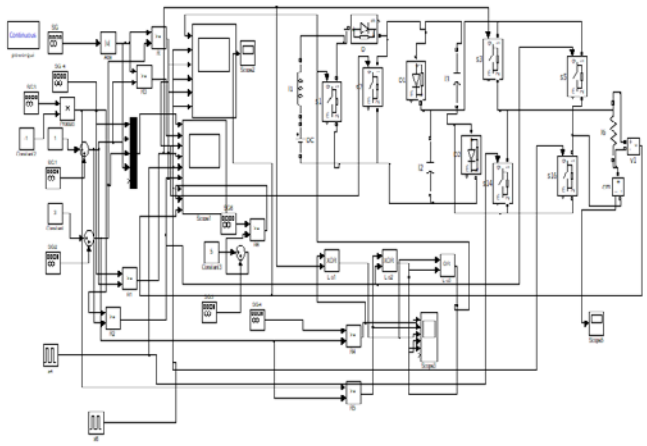

Fig.5. Simulink model of proposed MLI

Gate pulses for various switching devices S1, S2, S3, S4, S5 ,S6 are given in fig.6.

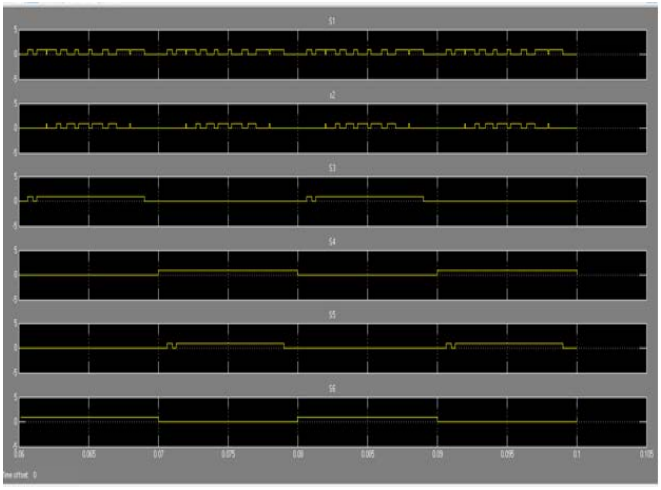

Fig.6. Gate pulses for various switching devices

Output voltage across load of the proposed 5 level inverter without filter is shown in fig.7.

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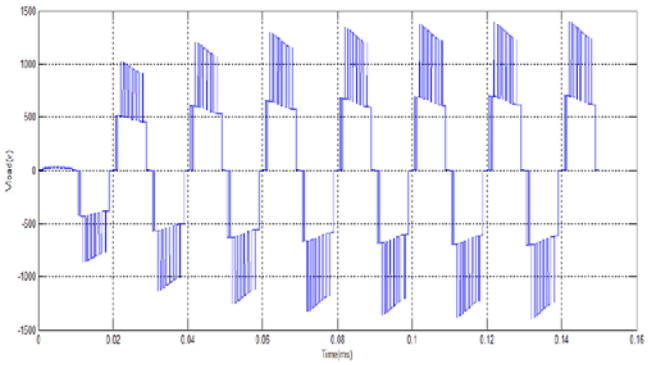

Fig.7. Output voltage across load of the proposed 5 level Inverter without filter

Load current of the proposed 5 level inverter without filter is shown in fig.8.

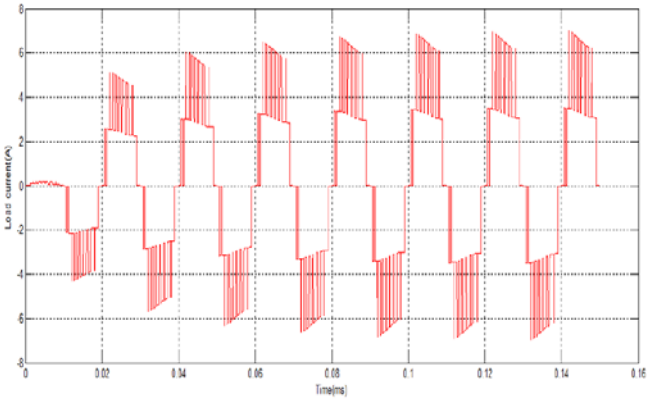

Fig.8. Load current of the proposed 5 level MLI without filter

THD of the Output voltage of the proposed boost converter based inverter without filter is shown in fig.9.

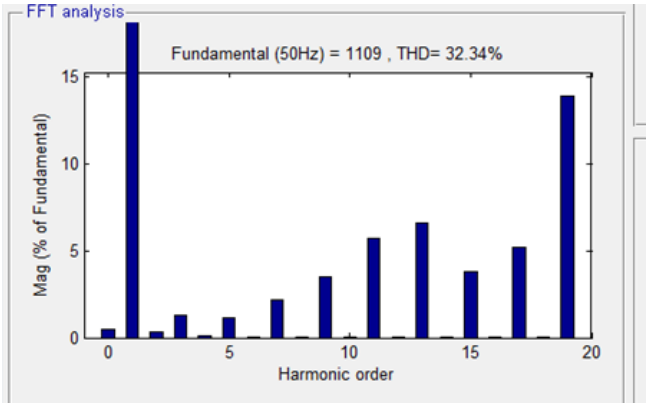

Fig.9. THD of the Output voltage of the proposed boost converter based Inverter without filter

Output voltage of the proposed MLI with filter is shown in fig.10.

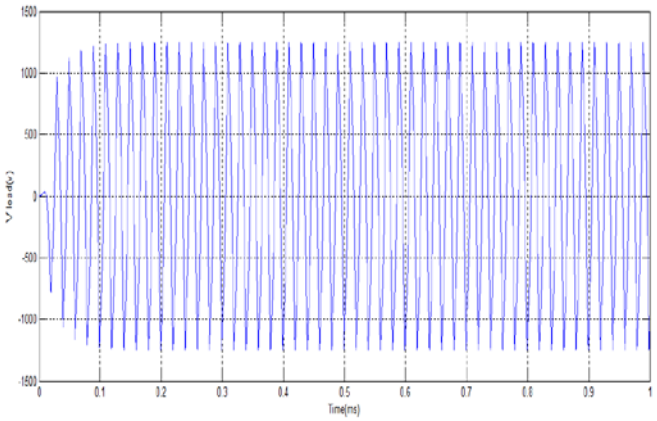

Fig.10. Output voltage of the proposed MLI with filter

The load current waveform of the proposed inverter with filter is shown below in fig.11.

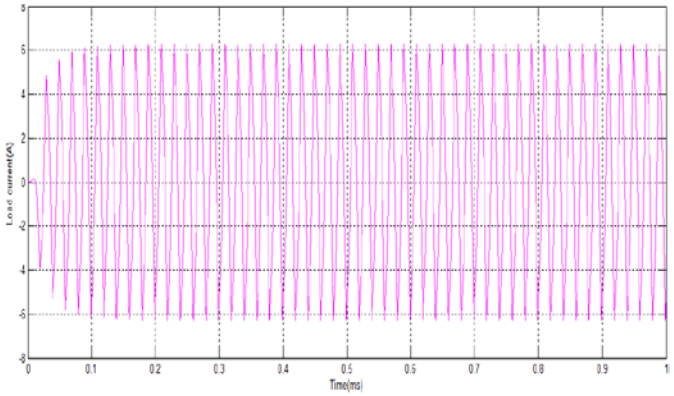

Fig.11. Load current waveform of proposed inverter with filter

THD of the Output voltage of the discussed single phase MLI with filter is shown in fig.12.

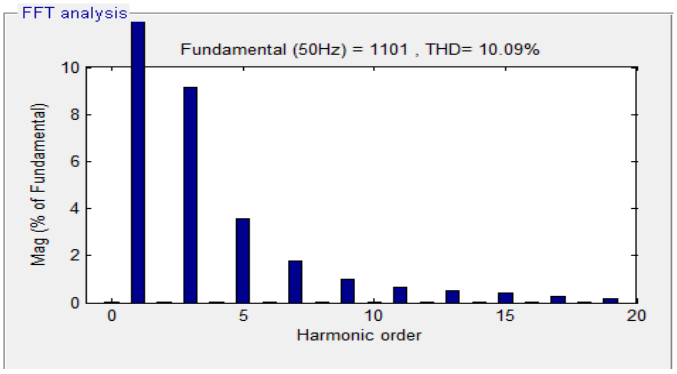

Fig.12. THD of the Output voltage of the proposed single phase Inverter with filter

Voltage across capacitances C1 and C2 and voltage available across polarity changing unit are shown below. Voltage across capacitances C1 and C2 are shown in fig.13.

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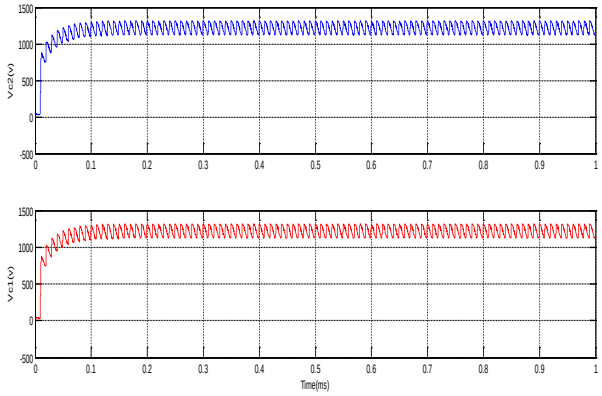

Fig.13. Voltage across capacitances C_1 and C_2

Voltage available across polarity changing unit is shown in fig.14.

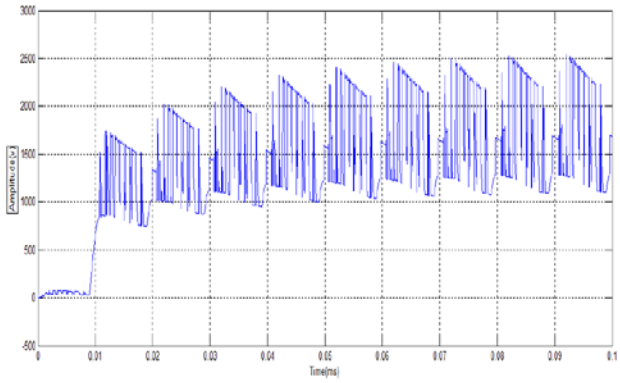

Fig.14. Voltage available across polarity changing unit

V. Conclusion

The proposed five level Inverter uses less no. of switches and a DC source compared to conventional 5 level inverters. Other DC sources are replaced by capacitors. In the suggested topology, 5 level inverter with and without filter are simulated in MATLAB/SIMULINK and their THD results were compared. Also by varying modulation indices V_{rms} and V_{peak} values were calculated and compared. In future, number of levels can be increased and the same work can be extended.

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