Implementation of Power and Delay Efficient SRAM Design

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Abstract - Based on Recent studies in memory systems ,peripheral circuits especially word line drivers constitute a large portion of the cache leakage. In addition as technology migrate to smaller geometries, leakage contribution to total power consumption increases faster than dynamic power, promoting leakage as the largest power consumption factor. In the past few years, numerous strategies have arisen for decreasing the chip size in SRAM. However with technology scaling it is becoming very difficult to maintain the better results for power reduction. In comparison with standard memory cells, the peripheral circuit dissipates excessive power. Power dissipation has become an important consideration for designing buffer because these circuits are not only amplifies the signal but also drive the large capacitive loads with high driving speed. For many designs optimization power is important for extended battery life of portable systems. The main objective of this paper is to reduce the power dissipation by exploiting CMOS taper buffer topology consisting of inverter stages which act as a word line drivers in SRAM design. The power and delay efficient SRAM has been designed using Cadence Virtuoso Analog design environment in 180nm technology.

Index Terms – *CMOS taper buffer, leakage power, sources of Power dissipation, SRAM design.*

I. INTRODUCTION

CMOS TAPERED BUFFER DESIGN

Low power has emerged as a principle theme in today's world of VLSI industries. This section presents concept of CMOS taper buffer design. The tapered buffer design consists of a chain of inverter stages where width of each MOS transistor in a stage is increased by a constant factor (called tapering factor) than that of the transistors placed on the previous stage. The constant increase in width of transistors in each stage provides fixed ratio of output current drive to output capacitance and hence equal rise, fall, and delay times for each stage[4].

Buffers are used to reduce the delays in driving high capacitive loads such as off-chip circuitry, clock drivers, bus drivers, etc. Lin and Linholm first introduced the CMOS tapered buffer in 1975 . The two important mathematical relations required to carry out the simulation and to calculate the results are technology dependent tapering factor and the number of buffer stages required. The technology dependent tapering factor (F) is given by

$F[\ln(F)-1] = C_d$

The number of buffer stages (N) required are given by,

$N = \ln(C_L/C_I) \ln F$

Here, C_d is the drain capacitance of minimum size inverter, C_L is the load capacitance, C_I is the input capacitance. The buffer circuits are used in variety of digital applications. A very common usage of these buffer is in memory devices[7].

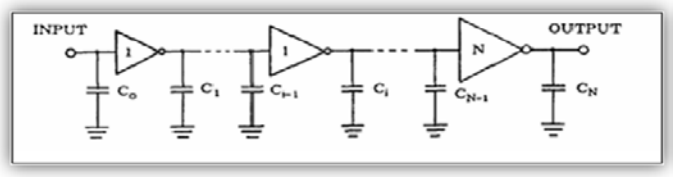

Figure 1:N stage taper buffer

Currently, CMOS VLSI is still advancing at a remarkable rate. A drawback of this trend lies in a continuing increase in leakage power dissipation. Recent results have shown that leakage in SRAM peripheral circuits such as word line drivers as well as input and output drivers are now the main sources of leakage.

II. LEAKAGE POWER DISSIPATION

Leakage power dissipation has become the dominant component of the total power dissipation in deep sub-micron technologies. A number of process and circuit techniques have been proposed to significantly reduce the leakage of the memory cell array in SRAMs. For instance, a word line driver drives its signal to a large number of memory cells. Given

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such a high capacitive load a chain of inverter buffers of increasing size is used, typically with three to five levels. In brief two main reasons explain this difference in leakage[1].

1. Memory cells are designed with minimal sized transistor mainly for area considerations. Unlike memory cells, peripheral circuits use larger, faster and accordingly more leaky transistors in order to satisfy timing requirements.

2.Memory cells use high threshold voltage transistors which have a significantly lower leakage reduction compared with typical threshold voltage transistors used in peripheral circuit

III.POWER DISSIPATION

This section explains about the Power dissipation and the sources of leakage currents. The basic power equation is

$$P = I \times V_{DD} \quad (1)$$

where I is the current flowing from V_{DD} to ground. The power dissipation in a CMOS tapered buffer has got three main components. These components are dynamic power ,short-circuit power , and leakage power . Short circuit power dissipation is assumed to be negligible in many designs, because NMOS and PMOS in the CMOS inverter remain ON for very short duration of time. It depends on the values of rise and fall time of applied signal thus we can control this power by controlling V_{th} and rise/fall time of input pulse. The total power dissipation is thus

$$P_{TOTAL} = P_{SHORT\ CIRCUIT} + P_{DYNAMIC} + P_{LEAKAGE} \quad (2)$$

$$P_{LEAKAGE} = I_{LEAKAGE} \times V_{DD} \quad (3)$$

$$P_{DYNAMIC} = C_L * V_{DD} * f \quad (4)$$

Where C_L is capacitive load, VDD is VDC applied and f is the frequency of operation. The leakage power is the power which is dissipated by Buffer in OFF state and it is the function of sub threshold leakage current and VDD applied to the drain terminal of MOS.

The main sources of leakage currents are :

1.Reverse biased junction leakage current

This occurs from source or drain to the substrate through reverse biased diodes when transistor is off.

2.Gate direct tunneling leakage

Reduction of gate oxide thickness results in an increase in the field across the oxide. This results in tunneling of electrons from substrate to gate and from gate to substrate through the gate oxide, resulting in gate oxide tunneling current.

3.Sub threshold leakage

The sub threshold leakage is a weak inversion conduction current that flows from source to the drain of the CMOS transistor when $V_{gs} < V_{th}$. It increases exponentially due to reduced threshold voltage, and is a main leakage component in high forward body bias . But if the value of V_{th} increases with RBB the sub threshold power gets reduced because it is the function of sub threshold leakage current in the idle state. Since reduction in V_{th} causes transistor sub threshold leakage current (I_{sub}) to increase exponentially and furthermore, other components of leakage current, e.g., the gate leakage and reverse-biased junction Band To Band Tunneling (BTBT) become important as we scale fabrication technology to 45 nm and downwards. RBB is a method which is employed in the proposed work to have variation in threshold voltage. If we adopt a strategy to adjust the transistors sizing using optimal values of primary factors such that its delay could be optimized then we can take the benefit of power minimization using reverse body biasing in Tapered buffers.

IV.CIRCUIT TECHNIQUE FOR LEAKAGE REDUCTION

Multiple threshold Designs: Multiple-threshold CMOS technologies, which provide both high and low threshold transistors in a single chip, can be used to deal with the leakage problem. The high-threshold transistors can suppress the sub threshold leakage current, while the low-threshold transistors are used to achieve high performance. Multiple-threshold voltages can be achieved by the following methods. a) Multiple channel doping. b) Multiple oxide CMOS ,c) Multiple channel length d) Multiple body bias. The Proposed design is based on multiple body bias.

V.PROPOSED BUFFER DESIGN

The proposed four stage buffer chain shown in figure 2 is the solution to reduce the static power dissipation. The modified buffer is the combination of four stage tapered buffer with bypass circuitry and reverse body biasing technique. The reverse body bias (RBB) is the type of Fixed Body Biasing scheme which is used to decrease the leakage current by increasing the threshold voltage V_{th} of the circuit[5] . Thus one can reduce the value of V_{th} while keeping the VDD constant. The reverse body bias technique is helpful to reduce leakage current of the idle portions of the logic circuits. Body biasing of NMOS has been implemented by giving low voltage (V_{SUB}=300mv) between body and the source terminals of Q1, Q2, Q3 and Q4 shown in figure 2. Body biasing can vary V_{TH} of a MOS without varying the value of V_{DD} . This improves the threshold voltage of the transistor, due to that leakage can be minimized. By using the reverse body biasing technique, the sub threshold leakage current can be reduced. This buffer will acts a word line driver in SRAM design.

The bypass circuitry shown in figure 2 which dissipates lesser power because where NMOS and PMOS is used as bypass and charging or discharges the output node in advance before input signal reached the output stage by stage. This reduces the power dissipation across load and propagation delay in a large manner because input signal need not to pass all the stages, it can easily bypassed directly to last stage. So switching of circuit becomes really fast that minimizes propagation delay[4].

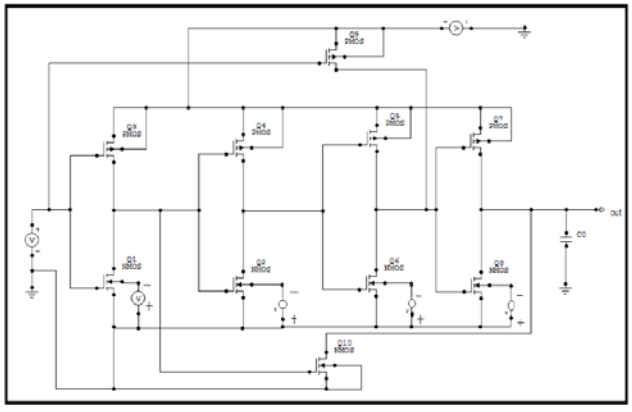

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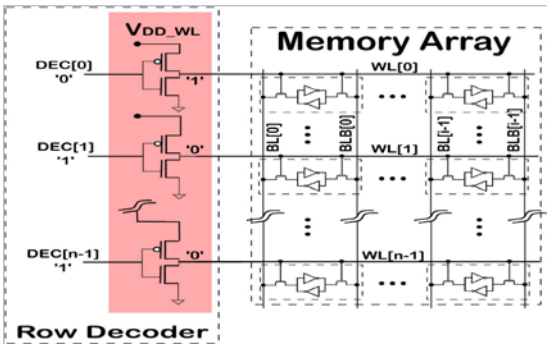
Figure 2:Proposed buffer design



Although this pre-charge logic scheme introduces additional transistors in the circuit in the form of bypass NMOS and PMOS but still this is very power efficient and optimized delay approach.

V.RESULTS AND ANALYSIS:

To carry out the simulations Cadence tool is used. The buffer proposed in this paper was evaluated and shown in table 1. Computations have been made by doing calculations for parameters like number of buffer stages (N) and technology dependent tapering factor (F). Both the designs have been compared on the basis of power dissipation. The figure 3 shows the schematic diagram of four stage conventional buffer which consists of four inverters.

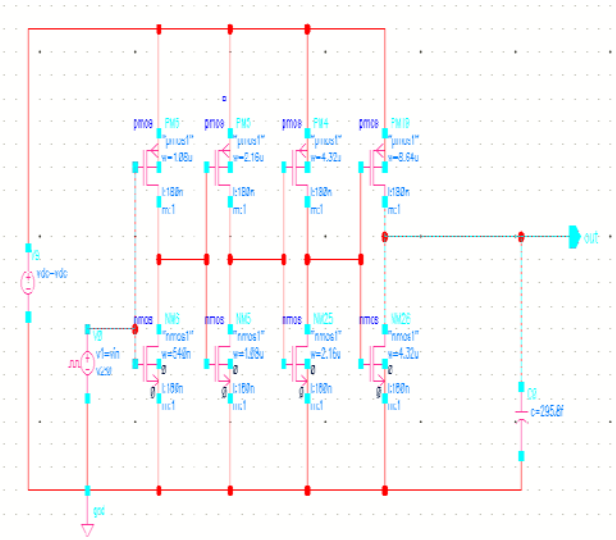


Figure 3:schematic of four stage conventional buffer

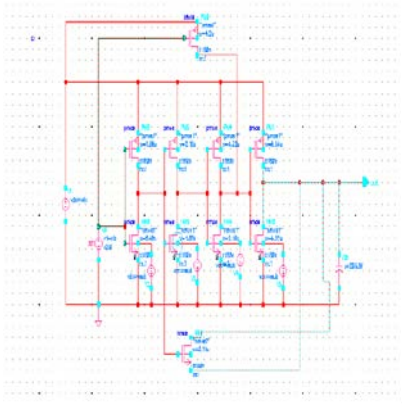


Figure 4:schematic of Proposed buffer

Figure 5:General block diagram of SRAM array

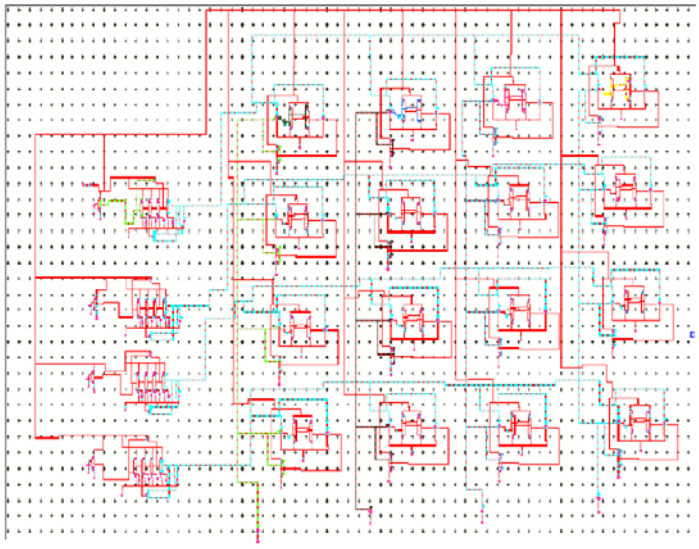


Figure 6:schematic of Proposed SRAM design

The proposed SRAM design consists of row decoder,word line drivers,SRAM cells.

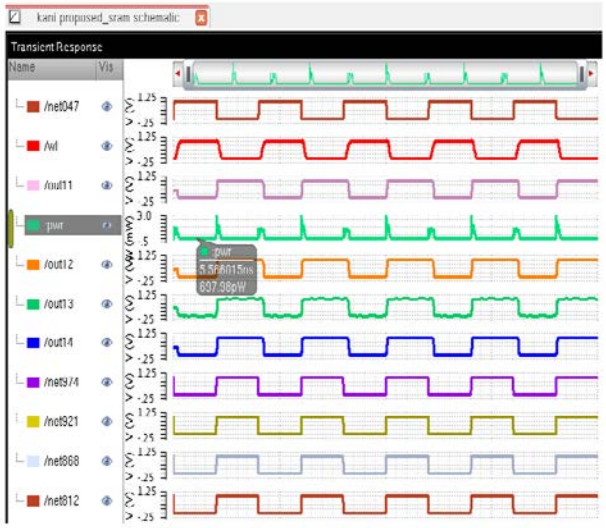


Figure 7:output waveform of proposed SRAM design

The figure 7 shows the output waveform of proposed SRAM design

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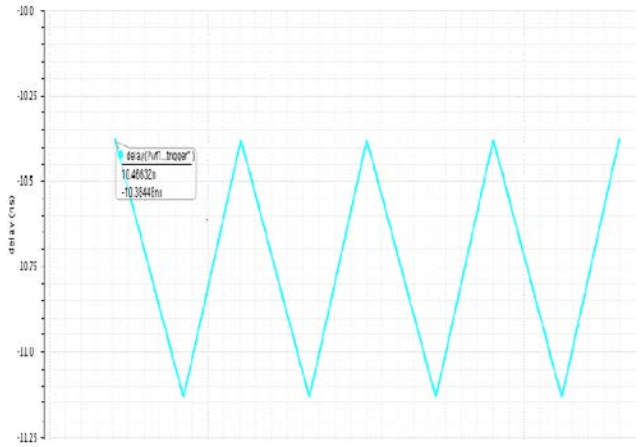

The figure 8 shows the delay waveform of proposed SRAM design

TABLE I COMPARISON FOR POWER DISSIPATION BETWEEN CONVENTIONAL SRAM DESIGN AND PROPOSED SRAM DESIGN

TOPOLOGY'S	STATIC POWER(pw)	AVERAGE LEAKAGE(uw)	DELAY(ns)
Conventional SRAM design	785.91	113.0	10.98
Proposed SRAM design	697.99	98.69	10.38

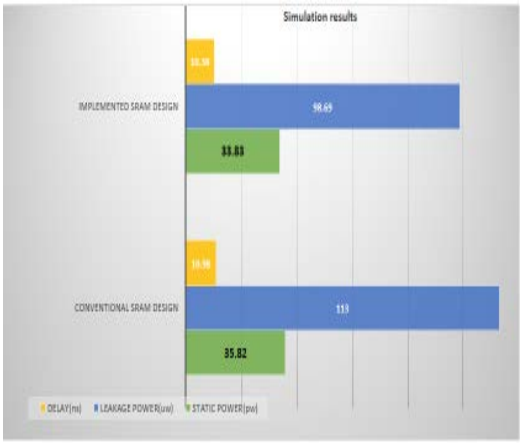

Chart 1:comparison of conventional SRAM and proposed SRAM

The chart 1 shows the comparison in terms of static Power, leakage power and delay between conventional And proposed SRAM design based on the values of TABLE I.

VI. CONCLUSION AND FUTURE WORK

In this paper, a circuit design is proposed and implemented to reduce leakage in SRAM memory peripheral circuits. The power reduction has been achieved by using bypass and reverse body biasing techniques. A leakage reduction of 14.31% in implemented SRAM design is achieved as compare to conventional SRAM design. Hence the SRAM can be designed and simulated using Cadence Virtuoso environment. The proposed work not only improves the performance parameters of Tapered Buffer but also provides the optimal value of V_{th} for which Buffer dissipates least Average power. This work can be extended in future with the use of mixed body biasing (FBB and RBB) in processor designs and achieve decrease in the leakage powers in Low Power Mode and decrease in the critical path delays in Active Mode of Operations. These projects can be further extended by using various Nanometer technologies like 135nm, 90nm, 45nm which are more dominantly used compared to 180nm technology in recent times.

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